

## **REMARKS/ARGUMENTS**

The Applicant originally submitted Claims 1-16 in the application. The Applicant has not amended, canceled or added any claims. Accordingly, Claims 1-16 are currently pending in the application.

### **I. Provisional Rejection of Claims 1-16 under Nonstatutory Double Patenting**

The Examiner has provisionally rejected Claims 1-16 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over copending Application No. 09/809,499. In response, the Applicants have filed a Terminal Disclaimer in compliance with 37 CFR 1.321(c) to overcome this provisional rejection. Accordingly, the Applicants respectfully request the Examiner to withdraw this objection and allow issuance thereof.

### **II. Rejection of Claims 1-16 under Nonstatutory Double Patenting**

The Examiner has rejected Claims 1-16 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-23 of U.S. Patent No. 6,353,896 to Holzmann, *et al.* (Holzmann). The Applicants respectfully disagree.

Holzmann provides a technique directed to the efficient testing of event driven software and making it possible to track the validity of future changes to the program code as part of the normal maintenance, extension and revision process to the source code. (See column 3, lines 16-21.) Holzmann, among other things, parses a source program to identify control states and converts the source program to a state machine format. A translation map is applied to the plurality of

instructions of the source program and the state machine format of the source program is converted to a verification program. (*See* claim 1.)

Holzmann does not claim, however, defining a control flow for procedures in a source code and populating the control flow with strings of a target language as recited in independent Claims 1, 10 and 11 of the present invention. Instead, as stated above, Holzmann converts source program to a state machine format and converts the state machine format to a verification program. Thus, Holzmann teaches a model extracting process that can be used as input to a logic model checker, whereas the present invention provides a more automatic method of extracting a verification model from source code by translating source strings generated from the source code into strings belonging to a target language. (*See* the Abstracts of Holzmann and the present invention.) Accordingly, for at least these reasons, the present invention is patentably distinct from Holzmann.

Since the present invention is patentably distinct from Holzmann, the Applicant respectfully requests the Examiner to withdraw the double-patenting rejection and allow issuance of Claims 1-16.

### **III. Rejection of Claims 1-12 and 15-16 under 35 U.S.C. §103**

The Examiner has rejected Claims 1-12 and 15-16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,625,797 to Edwards, *et al.* (Edwards) in view of U.S. Patent No. 5,615,137 to Holzmann, *et al.* (Holzmann 137). The Applicant respectfully disagrees.

Edwards is directed to electronic design automation and computer-aided hardware design. More specifically, Edwards is directed to a computer-based technique for compiling functional algorithmic descriptions written in a high-level software language into digital hardware

implementations. (*See* column 1, lines 8-12.) Edwards does not teach or suggest, however, extracting a verification model from source code comprising generating the verification model in a target language including populating a control flow of procedures in the source code with strings of the target language as recited in independent Claims 1 and analogously independent Claims 10 and 11. On the contrary, the Applicant does not find where Edwards even addresses extracting a verification model from source code. Instead, Edwards generates hardware representations of bytecode. (*See* column 6, lines 26-39.) The generated hardware is not a target language and, furthermore, is not generated by populating a control flow of procedures in the source code with strings of the target language. Thus, Edwards does not teach or suggest each element for which it has been cited.

Holzmann 137 is directed to verifying systems with concurrently-operating components. (*See* column 1, lines 11-14.) Holzmann 137 has not been cited to cure the above deficiencies of Edwards but to teach optimizing a model. (*See* Examiner's Office Action, page 5.) Nevertheless, Holzmann 137 also does not teach or suggest extracting a verification model from source code comprising generating the verification model in a target language including populating a control flow of procedures in the source code with strings of the target language as recited in independent Claims 1, 10 and 11. Holzmann 137 teaches a verification system where a system description and a description of a required property of the system description are input into a verifier generator that then generates a verifier. (*See* column 3, lines 37-49 and Figure 1.) Thus, Holzmann 137 teaches inputting a system description and a required property to generate a verifier instead of populating a control flow with strings of target language as claimed in the present invention. Accordingly, the

cited combination of Edwards and Holzmann 137 do not teach or suggest each and every element of independent Claims 1, 10 and 11.

Since the cited combination of Edwards and Holzmann 137, individually or in combination, fails to teach or suggest each element of independent Claims 1, 10 and 11, the cited combination does not provide a *prima facie* case of obviousness of Claims 1, 10 and 11 and Claims dependent thereon. Thus, Claims 1-12 and 15-16 are not unpatentable in view of the cited combination of Edwards and Holzmann 137. Accordingly, the Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §103(a) rejection of Claims 1-12 and 15-16 and allow issuance thereof.

Furthermore, the combination of Edwards and Holzmann 137 is improper since one skilled in the art would not be motivated to combine the teachings of Edwards and Holzmann 137. On the contrary, Edwards is directed to compiling software into a digital hardware implementation while Holzmann 137 is concerned with an efficient method of reducing state space for the benefit of “on the fly” verification tools of complex systems. (See the Abstract of Edwards and column 1, line 25 to column 2, line 23, of Holzmann 137.) While directed to efficiently representing algorithms with hardware (see column 2, lines 17-38), Edwards does not even teach or suggest verifying the algorithms that are represented by the hardware. Accordingly, Edwards provides no motivation to one skilled in the art to employ the digital hardware implementation of Edwards to model and verify complex systems.

#### **IV. Rejection of Claims 13-14 under 35 U.S.C. §103**

The Examiner has rejected Claims 1-12 and 15-16 under 35 U.S.C. §103(a) as being unpatentable over Holzmann 137, Edwards and in further view of U.S. Patent No. 6,389,385 to King. The Applicant respectfully disagrees.

King is directed to a safe system and a method for reversibly translating source code between unlike character sets. (*See* column 1, lines 6-10.) King has not been cited to cure the deficiencies of Edwards and Holzmann 137 but to teach the subject matter of dependent Claims 13-14. (*See* Examiner's Office Action, pages 14-15.) Thus, the cited combination of Edwards, Holzmann 137 and King does not teach each element of independent Claim 11 and does not provide a *prima facie* case of obviousness of Claims 13-14 which depend thereon. Thus, Claims 13-14 are not unpatentable in view of the cited combination of Edwards, Holzmann 137 and King. Accordingly, the Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §103(a) rejection of Claims 13-14 and allow issuance thereof.

#### **V. Comment of Cited References**

The Applicant reserves further review of references cited but not relied upon if relied upon in the future.


## VI. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-16.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, P.C.

A handwritten signature in black ink, appearing to read "J. Joel Justiss". The signature is fluid and cursive, with a large initial "J" and a long horizontal stroke extending to the right.

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